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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/499,060	02/04/2000	Christophe Garnier	98GR22045417	9699

27975 7590 11/17/2004

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EXAMINER	
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ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/17/2004

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/499,060
Filing Date: February 04, 2000
Appellant(s): GARNIER ET AL.

Michael W. Taylor
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 08/20/04.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is incorrect. A correct statement of the status of the claims, responsive to the amendment filed 23 September 2004, is as follows:

This appeal involves claims 9-20, 36, 37 and 40.

Claims 21, 24-30 and 32-35 are allowed.

Claims 1-8, 22, 23, 31 and 38-39 have been canceled.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is incorrect. The statement discusses all amendments, not the amendments After-Final. Further, such does not include the amendment filed after the Appeal Brief.

The amendment after final rejection filed on 23 September 2004 has been entered.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct, for similar reasons as discussed above. The changes are as follows:

The issue on appeal is whether Claims 9-20, 36, 37 and 40 are unpatentable under 35 U.S.C. §103 over the Appellants' prior art Fig. 1 in view of Tanigawa (U.S. Patent No. 4,814,724) and Lauffenburger (U.S. Patent No. 5,254,957).

(7) Grouping of Claims

The rejection of claims 9-20, 36, 37 and 40 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

Applicant's Prior Art Fig. 1.

5,254,957	Lauffenburger	10-1993
4,814,724	Tanigawa	03-1989

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-20, 36, 37 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art Fig. 1 in view of Tanigawa (USPN 4,814,724) and Lauffenburger (USPN 5,254,957).

Applicant's prior art Fig. 1 discloses a ramp generator comprising: "a capacitance (C)" and a "charging circuit (remainder of the circuit) connected to said capacitance". The "charging circuit" of Fig. 1 has a broad current source Ig1 with no expressed teachings of the structure thereof. The reference to Tanigawa discloses in Fig. 4 a specific current sink comprising a "current generator (9)" having a "first resistance (the internal resistance of current source 9) and a "circuit (Q1, Q2 and R)" having "a second resistance (R)" and "current mirror (Q1 and Q2)". The circuit to Tanigawa is disclosed as having the advantage of gain control. It is notoriously well known that to modify a current sink circuit (the circuit of Fig. 4 of Tanigawa being a current sink) to a current source circuit, such requires changing the conductivity types of the transistors and the polarities of the power supply. Reference is made to Figs. 8 and 9 of Lauffenburger which demonstrates the notoriety of this modification. Therefore, it would have been obvious for one skilled in the art to modify the circuit of Fig. 4 of Tanigawa to be a current source circuit by changing the conductivity types of the transistors (change Q1 and Q2 to PNP) and the polarities of the power supply (i.e. swap Vcc and ground) as is notoriously well known in the art as disclosed by Lauffenburger. Further, it would have been obvious for one skilled in the art to use the specific current source of Tanigawa, modified as discussed above, for the broad current source Ig1 of Applicant's prior art Fig. 1 for the expected advantage of obtaining a constant current with gain control.

Additionally, in the reference to Tanigawa there is no specific discussion of MOS transistors. However, it is notoriously well known that bipolar transistors and MOS transistors are art-recognized equivalents. Additionally, it is notoriously well known that MOS transistors have reduced leakage current as compared to bipolar transistors. Therefore, it would have been obvious for one skilled in the art to use MOS transistors in place of the bipolar transistors of Tanigawa in the above-modified circuit due to the doctrine of art-recognized equivalents and to obtain the expected advantage of reduced leakage current.

Additionally, Applicant's prior art Fig. 1 and the reference to Tanigawa do not expressly disclose that the circuit is "integrated". Examiner initially contends that "integrated" would be understood to merely mean, giving such its broadest reasonable interpretation, that the circuit elements are together. Clearly, the elements in the above combination are together. However, Examiner further contends that it is notoriously well known and customary to provide the circuit in integrated circuit form (i.e., provided together on a semiconductor) and that such will provide the well-known advantage of matching temperature response characteristics. This well-known advantage is expressly disclosed in Col. 3, lines 21-25, of Lauffenburger. Therefore, it would have been obvious for one skilled in the art to provide the above combination of Applicant's prior art Fig. 1 in view of Tanigawa and Lauffenburger in integrated form to obtain the expected advantage of matched temperature response characteristics.

Since the modified circuit includes MOS transistors and since Tanigawa discusses that resistor R is variable, it is clear that the resistor R can be varied such that the circuit will have the claimed operation. Examiner further contends that since transistor Q2 is modified to be a diode-connected MOS transistor, such will operate as a diode. As is well known, by having a diode

voltage drop, such will have a gate-to-source voltage substantially equal to the threshold voltage thereof. This will provide that the VGST-Vth will be negligible (i.e., almost zero). Thus, it would be true that Re x Ig2 >> VGT-Vth (as discussed in line 6 of page 6 of specification) for elements 9, Q2 and R of Tanigawa. As a result, the above modification will have the claimed operation of the "capacitance charging current" being "proportional to a square of a ratio of the second resistance (R) and the first resistance (resistance of 9)".

(11) Response to Argument

Initially, Examiner points out that the above modification including the combination of the references to Applicant's prior art Fig. 1, Tanigawa and Lauffenburger results in a circuit having identical structure to that presently claimed. This fact has not been contested in this Appeal.

The discussion on pages 4-6 discusses the claim language but does not provide any argument concerning the rejection.

The discussion at the end of page 6 through page 7 discusses the rejection but does not provide any substantive arguments.

In the paragraph linking pages 7 and 8, Appellant remarks that "In respect to the Examiner's position stated above, the Appellants' respectively submit that it is not necessarily true that Re x Ig2 >> VGST4-Vth4 for elements **9** and **Q2** of Tanigawa. According to the present invention, resistance **Re** is chosen so that Re x Ig2 >> VGST4-Vth4". In the following paragraph, Appellant again reiterates the importance of the value of Re being selected to provide the desired operation. Responsive to the arguments subsequently provided, Examiner contends that the combination provided in the rejection will provide the claimed operation.

In the paragraph linking pages 8-9, Appellant discusses the operation disclosed in the reference to Tanigawa which provides the relationship that $I_2 - I_1 \cdot A$, wherein "A is based upon the equation exp (V_{BE}/V_T). As provided in Tanigawa, I_1 is the current through transistor 9, Q2 and R, that I_2 is the current provided by Q1 and that V_T is the thermal voltage. Appellant further cites the portion of Tanigawa stating "the current I_2 is set to a value A times larger than the input current I_1". Appellant than concludes in the first full paragraph of page 9 that:

> "Tanigawa thus fails to teach or suggest that the capacitance charging current is proportion to a square of the ratio of the second resistance and the resistance, as resisted in independent Claim 9, for example"

From this argument, it appears that Appellant is contending that since I_2 is "larger" than I_1 (i.e., rather than them being equal), the base-emitter voltage of Q2 will not be substantially the same as the threshold voltage of Q2. However, Appellant failed to discuss the remainder of the citation that states:

> "Namely, by changing the values of the variable resistor R to vary the voltage thereacross, the gain of the amplifier circuit of the current mirror circuit type is set to any desired value."

This portion of the reference to expressly states that the gain can be "set to any desired value". This would clearly include a gain of one (i.e., A = 1). With a gain of one, the base-emitter voltage of Q2 will be substantially the same as the threshold voltage of Q2.

Further, Appellant is clearly using the entirely wrong analysis. The modification in the rejection expressly provides for using MOS transistors, not bipolar transistors. The equations provided Col. 1 of Tanigawa are for bipolar transistors only. As would be well understood by one skilled in the art and as disclosed in the specification, MOS transistors use entirely different equations than bipolar transistors to represent the characteristics. In the last line of page 5 of the

specification, an equation is provided that is true for all circuits having the structure with MOS transistors provided in Figs. 2 and 3. The specification then goes on to show operation of the circuit wherein the gate-source voltage (VGST4) of T4 is substantially the same as the threshold voltage (Vth4) of T4. This will provide a situation wherein "Re x Ig2 >> VGST4 - Vth4" (see line 6 of page 6). (Examiner notes, although not related to this Appeal, it is understood that "VGST5-Vth5 ≠ Re x Ig2", in line 7 of page 6 should be --VGST5-Vth5 ≈ Re x Ig2--.) Since the combined references, as modified in the rejection, will provide a circuit having the same structure as that recited in the claims, such will have this characteristic. Therefore, to obtain the claim language reciting "enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance", it is required that the value of the resistor, resistor R in Tanigawa, be set accordingly, as argued by Appellant.

Examiner contends that the claim language "enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance" is functional language. The reference to Tanigawa expressly discloses that resistor R is variable. Thus, it is seen that resistor R can be set to any value. Consistent with the findings established in *In re* Swinehart, 169 USPQ 226 (CCPA 1971) and *In re* Schreiber 44 USPQ2d 1429 (Fed. Cir. 1997), Examiner contends that the circuit combination provided in the rejection is capable of providing the claimed function due to resistor R being variable.

Additionally, Examiner again points to the portion of the reference to Tanigawa, discussed above, which states that the value of resistor R can by varied to provide a gain of "any desired value". The ability of adjusting R to obtain any "desired" gain would be seen by one skilled in the art to include adjusting R such that the gate-source voltage (VGST4) of the MOS

transistor for Q2 is substantially the same as the threshold voltage thereof. Upon meeting this condition, it is clear that the current provided at I2 will be "proportional to a square of a ratio of the second resistance (R) and the first resistance (resistance of 9)".

In the last two paragraphs of page 9, Appellant discusses that the circuit claimed is in "CMOS technology" and the advantages thereof.

In the first two paragraphs of page 10, Appellants provides arguments that the circuit of Tanigawa cannot be integrated by pointing to a portion of the reference in Col. 2 and concludes "the 'second' resistance R in Tanigawa is not produced in CMOS technology". However, the reference to Tanigawa was published on 21 March 1989. Reference is made to the above cited basis for the rejection under 35 U.S.C. § 103 which states "A patent may not be obtained...if the differences...would have been obvious at the time the invention was made" (emphasis added), not the time of the applied references. The filing date of the instant application is 04 February 2000. The rejection provided above expressly provides why the combination would have been obvious "at the time the invention was made". Integration of resistor elements was well known to have been common at the time of the invention. This is clearly established in the discussion of the prior art in the specification.

Additionally, the claim does not require that the "second resistor" R is "produced in CMOS technology". The claim states that the circuit is "produced using CMOS technology" and that the "charging circuit" is "CMOS". There is no express requirement in the claims that either the "first resistor" or the "second resistor" be "CMOS". By reciting that the circuit is "produced using CMOS technology" and that the "charging circuit" is "CMOS", such would be interpreted by one skilled in the art to only require that a portion of the "charging circuit" is "CMOS".

Clearly, since the modification requires MOS transistors for Q1 and Q2, it would be seen more than reasonable that the circuit is "produced using CMOS technology".

In response to the arguments in the remainder of the Brief, Examiner responds that the reference to Lauffenburger is not relied upon in the above rejection for the teaching concerning the discussed functional language.

In the first full paragraph of page 11, Appellant again argues that the combination does not provide the recited function. However, reference is made to the above comments establishing that the circuit of the combined references anticipates that claim language and/or would be capable or providing this functional language.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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November 10, 2004

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